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RareBooksClub. Paperback. Book Condition: New. This item is printed on demand. Paperback. 66 pages. Original publisher: Aberdeen Proving Ground, MD : Army Research Laboratory, 1999 OCLC Number: (OCoLC)311097378 Subject: Computational fluid dynamics. Excerpt: . . . This report will discuss how this effect was SGI Power Challenge and on the Convex Exemplar approached, what the results were, and the reasons for those results. 2. The Architecture of the SGI Power Challenge Before one can discuss the results of this effort, it is helpful to have a short introduction to the architecture involved. The SGI Power Challenge can be thought of as the prototypical RISC-based cache-coherent shared memory SMP. As such, it will be discussed first. From the hardware perspective, it has the following properties: (1) Powerful RISC-based processors. In this case, R5000 processors rated at 300 MFLOPS each. (2) This version of the Power Challenge had up to 18 processors and up to 16 GB of memory, although one could not configure a system with both 18 processors and 16 GB of memory. (3) Each processor had a large on-chip cache (4 MB). (4) Hardware protocols maintain the coherency between all of the caches and main memory. This is a key requirement if shared memory is to be implemented entirely in hardware. (5) Shared memory is entirely implemented in hardware. All of the boards are connected by a common system bus that implements a snoopy bus protocol for cache coherency. This bus gives a The speed of the bus is a key limiting factor in uniform memory access time. determining how many processors can run in a system at one time without running out of memory bus bandwidth. This item ships from La Vergne, TN. Paperback.



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